



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

GARG *et al.*

Appl. No.: 10/060,086

Filed: January 31, 2002

For: **RISC Microprocessor Architecture  
Implementing Multiple Typed  
Register Sets**

Confirmation No.: 6414

Art Unit: 2154

Examiner: Larry D. Donaghue

Atty. Docket: 2047.0600007

**Second Supplemental Information Disclosure Statement**

***Mail Stop Amendment***

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Sir:

Listed on accompanying IDS Forms are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

03/27/2006 HALI11 00000018 10060086  
01 FC:1806 180.00 DP

- ☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.
- ☐ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- ☒ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.
- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than

three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☒ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of \$180.00 in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of \$\_\_\_\_\_ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than

three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

- ☒ 5. Documents **FP1-FP8** were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report, **NPL12**, that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

Documents **FP1**, **FP2**, **FP5** and **FP7** were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report, **NPL13**, that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

Documents **FP1**, **FP5**, and **FP9-FP11** were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report, **NPL14**, that indicates the degree of

relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

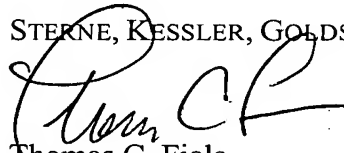
- ☐ 6. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).
- ☒ 7. Copies of documents **FP1-FP11** and **NPL1-NPL14** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents and patent application publications cited on the attached IDS Forms are submitted.
- ☒ 8. Copies of documents **FP12-FP16** and **NPL15-NPL70** were previously submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in the present Application on December 3, 2002. Thus, copies of these documents are not attached.
- ☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent application no(s). 09/840,026 in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



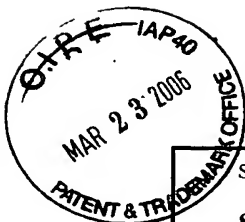
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Attorney for Applicants  
Registration No. 43,610

Date:

3/23/06

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<b>Substitute for form 1449/PTO</b>  <b>SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(Use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	10/060,086
				Filing Date	January 31, 2002
				First Named Inventor	Sanjiv GARG
				Art Unit	2154
				Examiner Name	Larry D. Donaghue
Sheet	1	of	9	Attorney Docket Number	2047.0600007

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
	US1	5,125,092	06/23/1992	Prener	
	US2	5,214,786	05/25/1993	Watanabe et al.	
	US3	5,133,077	07/21/1992	Karne et al.	
	US4	5,093,783	03/03/1992	Kitada	
	US5	07/259,345	10/18/1988	Barbour	
	US6	4,128,880	12/1978	Cray, Jr.	
	US7	4,212,076	07/1980	Connors	
	US8	4,626,989	12/1986	Torii	
	US9	4,675,806	06/1987	Uchida	
	US10	4,722,049	01/1988	Lahti	
	US11	4,807,115	02/1989	Torng	
	US12	5,125,092	06/1992	Prener	
	US13	5,201,056	04/1993	Daniel et al.	
	US14	5,226,126	07/1993	McFarland et al.	
	US15	5,230,068	07/1993	Van Dyke et al.	
	US16	5,241,636	08/1993	Kohn	
	US17	5,442,757	08/1995	McFarland et al.	
	US18	5,487,156	01/1996	Popescu et al.	
	US19	5,493,687	02/1996	Garg et al.	
	US20	5,560,035	09/1996	Garg et al.	

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		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
	FP1	JP 2-226342	09/07/1990			
	FP2	JP-A-62-242243	10/22/1987			
	FP3	JP-A-1-142831	06/05/1989			
	FP4	JP-A-1-199233	08/10/1989			
	FP5	JP-A-60-144830	07/31/1986			
	FP6	JP-A-61-40650	02/26/1986			
	FP7	JP-A-2-118757	05/07/1990			
	FP8	JP-A-2-224025	09/06/1990			
	FP9	JP 2-211534	08/22/1990			
	FP10	JP 57-57345	04/06/1982			
	FP11	JP-3-35324	02/15/1991			

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449/PTO  <b>SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(Use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	10/060,086
				Filing Date	January 31, 2002
				First Named Inventor	Sanjiv GARG
				Art Unit	2154
Examiner Name	Larry D. Donaghue				
Sheet	2	of	9	Attorney Docket Number	2047.0600007

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		Number-Kind Code <sup>2</sup> (If Known)			
	US21	5,561,776	10/1996	Popescu <i>et al.</i>	
	US22	5,592,636	01/1997	Popescu <i>et al.</i>	
	US23	5,625,837	04/1997	Popescu <i>et al.</i>	
	US24	5,627,983	05/1997	Popescu <i>et al.</i>	
	US25	5,682,546	10/1997	Garg <i>et al.</i>	
	US26	5,708,841	01/1998	Popescu <i>et al.</i>	
	US27	5,768,575	06/1998	McFarland <i>et al.</i>	
	US28	5,797,025	08/1998	Popescu <i>et al.</i>	
	US29	5,832,293	11/1998	Popescu <i>et al.</i>	
	US30	5,838,986	11/1998	Garg <i>et al.</i>	
	US31	6,044,449	03/2000	Garg <i>et al.</i>	
	US32	6,249,856 B1	06/2001	Garg <i>et al.</i>	
	US33	2001/0034823 A1	10/2001	Garg <i>et al.</i>	
	US34				
	US35				
	US36				
	US37				
	US38				
	US39				
	US40				

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		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
	FP12	EP 0 170 284 A2	02/1986			
	FP13	EP 0 213 843 A2&A3	03/1987			
	FP14	EP 0 241 909 A2	10/1987			
	FP15	EP 0 454 636 A1	10/1991			
	FP16	GB 2 190 521 A	11/1987			
	FP17					
	FP18					
	FP19					
	FP20					
	FP21					

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				First Named Inventor	Sanjiv GARG
				Art Unit	2154
				Examiner Name	Larry D. Donaghue
Sheet	3	of	9	Attorney Docket Number	2047.0600007

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume issue number(s), publisher, city and/or country where published	T <sup>2</sup>
	NPL1	Patent Abstracts of Japan, Publication No. 02-226342, English Language Abstract for JP Patent Application No. 02-001127, (1 page).	
	NPL2	Patent Abstracts of Japan, Publication No. 62-242243, English Language Abstract for JP Patent Application No. 61-085442, (2 pages).	
	NPL3	English Language Abstract for JP Patent Publication No. 1-142831, (1 page).	
	NPL4	English Language Abstract for JP Patent Publication No. No. 1-199233.	
	NPL5	Patent Abstracts of Japan, Publication No. 60-144830, English Language Abstract for JP Patent Application No. 59-000424, (2 pages).	
	NPL6	Patent Abstracts of Japan, Publication No. 61-40650, English Language Abstract for JP Patent Application No. 59-163061, (1 page).	
	NPL7	Patent Abstracts of Japan, Publication No. 2-118757, English Language Abstract for JP Patent Application No. 63-271010, (2 pages).	
	NPL8	Patent Abstracts of Japan, Publication No. 2-224025, English Language Abstract for JP Patent Application No. 01-270136, (1 page).	
	NPL9	Patent Abstracts of Japan, Publication No. 02-211534, English Language Abstract for JP Patent Application No. 01-031652, (2 pages).	
	NPL10	Patent Abstracts of Japan, Publication No. 57-057345, English Language Abstract for JP Patent Application No. 55-132633, (2 pages).	

Examiner Signature		Date Considered	
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<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Sheet	4	of	9	Attorney Docket Number	2047.0600007

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T <sup>2</sup>
	NPL11	English Language Abstract for JP Patent Publication No. 3-35324, (1 page).	
	NPL12	Japanese language copy of the Notice of Rejection and the English language translation, issued by the Japanese Patent Office in Appl. No. 5-502403, dated July 22, 2003 (10 pages).	
	NPL13	Japanese language copy of the Notice of Rejection and the English language translation, issued by the Japanese Patent Office in Appl. No. 5-502403, dated March 2, 2004 (9 pages).	
	NPL14	Japanese language copy of the Notice of Rejection and the English language translation, issued by the Japanese Patent Office in Appl. No. 2004-010369, dated June 1, 2005 (9 pages).	
	NPL15	Acosta, R. D. et al., "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," <i>IEEE Transactions On Computers</i> , IEEE, Vol. C-35, No. 9, September 1986, pp. 815-828.	
	NPL16	Adams, R.G. et al., "Utilising low level parallelism in general purpose code: the HARP project," <i>Microprocessing and Microprogramming</i> , Elsevier Science Publishers, B.V., Vol. 29, No. 3, October 1990, pp. 137-149.	
	NPL17	Agerwala, T. and Cocke, J., A High Performance Reduced Instruction Set Processors, IBM Research Division, March 31, 1987, pp. 1-61.	
	NPL18	Aiken, A. and Nicolau, A., "Perfect Pipelining: A New Loop Parallelization Technique*," <i>ESOP '88, 2nd European Symposium on Programming</i> , Springer, ISBN 3-540-19027-9, 1988, pp. 221-235.	
	NPL19	Albert, A.J., "User Configurable Local Storage Registers," <i>IBM Technical Disclosure Bulletin</i> , IBM, Vol. 18, No. 12, May 1976, pp. 3971-3975.	
	NPL20	Birman, M. et al., "Design of a High-Speed Arithmetic Datapath," <i>Proceedings 1988 IEEE International Conference on Computer Design: VLSI in Computers &amp; Processors</i> , IEEE, October 3-5, 1988, pp. 214-216.	

Examiner Signature		Date Considered	
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Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T <sup>2</sup>
	NPL21	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," Computer, IEEE, Vol. 14, September 1981, pp. 18-27.	
	NPL22	Colwell, R.P. et al., "A VLIW Architecture for a Trace Scheduling Compiler," Proceedings of the 2nd International Conference on Architectural Support for Programming Languages and Operating Systems, ACM, October 1987, pp. 180-192	
	NPL23	Foster, C.C. and Riseman, E.M., "Percolation of Code to Enhance Parallel Dispatching and Execution," IEEE Trans. On Computers, IEEE, December 1971, pp. 1411-1415.	
	NPL24	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," Proceedings of the 2nd International Conference on Supercomputing, ACM Press, 1988, pp. 442-452	
	NPL25	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," Proceedings of the 2nd International Conference on Supercomputing, ACM Press, 1988, pp. 442-452	
	NPL26	Gross, T.R. and Hennessy, J.L., "Optimizing Delayed Branches," <i>Proceedings of the 5th Annual Workshop on Microprogramming</i> , IEEE, October 5-7, 1982, pp. 114-120.	
	NPL27	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," COMPCON 90: 35th IEEE Computer Society International Conference, IEEE, Feb. 26, 1990, pp. 166-172.	
	NPL28	Horst, R.W. et al., "Multiple Instruction Issue in the NonStop Cyclone Processor," Proceedings of the 17th Annual International Symposium on Computer Architecture, ACM Press, 1990, pp. 216-226.	
	NPL29	Hunter, C., Series 32000 Programmer's Reference Manual, Prentice-Hall Inc., Englewood Cliffs, NJ, 1987, pp. 2-4, 2-21, 2-23, 6-14 and 6-126.	
	NPL30	Hwang, K. and Briggs, F.A., Computer Architecture and Parallel Processing, McGraw-Hill, 1984, pp. 264-280.	

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Substitute for form 1449/PTO				<b>Complete if Known</b>	
<b>SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use as many sheets as necessary)				Application Number	10/060,086
				Filing Date	January 31, 2002
				First Named Inventor	Sanjiv GARG
				Art Unit	2154
				Examiner Name	Larry D. Donaghue
Sheet	6	of	9	Attorney Docket Number	2047.0600007

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T <sup>2</sup>
	NPL31	Hwu, W. W. and Patt, Y.N., "Checkpoint Repair for High-Performance Out-of-Order Execution Machines," IEEE Transactions On Computers, IEEE, Vol. C-36, No. 12, December 1987, pp. 1496-1514.	
	NPL32	Hwu, W.W. and Chang, P.P., "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," Proceedings of the 15th Annual Symposium on Computer Architecture, IEEE, June 1988, pp. 45-53.	
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	NPL34	IBM Journal of Research and Development, IBM, Vol. 34, No. 1, January 1990, pp. 1-70.	
	NPL35	Johnson, W. M., Super-Scalar Processor Design, (Dissertation), Copyright 1989, 134 pages.	
	NPL36	Jouppi, N.P. and Wall, D.W., "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," Proceedings - 3rd International Conference on Architectural Support for Programming Languages and Operating Systems, ACM Press, April 1989, pp. 272-282.	
	NPL37	Jouppi, N.H., "Integration and Packaging Plateaus of Processor Performance," International Conference of Computer Design, IEEE, October 2-4, 1989, pp. 229-232.	
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	NPL39	Kanai, T. et al., "A 16-bit Microcomputer FPD70423 for Serial Communication," NEC Research & Development, NEC, Vol. 32, No. 3, July 1991, pp. 350-360.	
	NPL40	Keller, R.M., "Look-Ahead Processors," Computing Surveys, ACM, Vol. 7, No. 4, December 1975, pp. 177-195.	

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	NPL41	Kogge, P.M., The Architecture of Pipelined Computers, Hemisphere Publishing, 1981, pp. 167-172.	
	NPL42	Lam, M.S., "Instruction Scheduling For Superscalar Architectures," Annu. Rev. Comput. Sci., Annual Reviews, Inc., Vol. 4, 1990, pp. 173-201.	
	NPL43	Lee, R.B., "Precision Architecture," IEEE Computer, IEEE, pp. 78-91, January 1989.	
	NPL44	Maejima, H. et al., "A 16-bit Microprocessor with Multi-Register Bank Architecture," Proc. Fall Joint Computer Conference, IEEE, Nov. 2-6, 1986, pp. 1014-1019.	
	NPL45	Margulis, N., "i860 microprocessor internal architecture," Microprocessors and Microsystems, Butterworth & Co. Ltd., Vol. 14, No. 2, March 1990, pp. 89-96.	
	NPL46	Miller et al., "Exploiting Large Register Sets," Microprocessors and Microsystems, Butterworth-Heinemann Ltd., Vol. 14, No. 6, July 1990, pp. 333-340.	
	NPL47	Molnar, K. et al., "A 40 MHz 64-Bit Floating-Point Co-Processor," 1989 IEEE International Solid-State Circuits Conference, IEEE, February 1989, pp. 48, 49 and 287.	
	NPL48	Murakami, K. et al., "SIMP (Single Instruction stream/Multiple instruction Pipelining): A Novel High-Speed Single-Processor Architecture," Proceedings of the 16th Annual International Symposium on Computer Architecture, ACM Press, 1989, pp. 78-85.	
	NPL49	Odnert, D. et al., "Architecture and Compiler Enhancements for PA-RISC Workstations," COMPCON Spring '91 digest of papers, IEEE, 1991, pp. 214-218.	
	NPL50	Patt, Y.N. et al., "Critical Issues Regarding HPS, A High Performance Microarchitecture," Proceedings of the 18th Annual Workshop on Microprogramming, ACM, December 1985, pp. 109-116.	

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	NPL51	Patt, Y.N. et al., "HPS, A New Microarchitecture: Rationale and Introduction," Proceedings of the 18th Annual Workshop on Microprogramming, ACM, December 1985, pp. 103-108.	
	NPL52	Patterson, D. A. and Séquin, C.H., "A VLSI RISC," Computer, IEEE, Vol. 15, No. 9, September 1982, pp. 8-18 and 20-21.	
	NPL53	Pleszkun, A.R. and Sohi, G.S., "The Performance Potential of Multiple Functional Unit Processors*," Proceedings of the 15th Annual Symposium on Computer Architecture, IEEE, June 1988, pp. 37-44.	
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	NPL55	Russell, R.M., "The CRAY-1 Computer System," Communications of the ACM, ACM, Vol. 21, No. 1, January 1978, pp. 63-72.	
	NPL56	Smith, M.D. et al., "Boosting Beyond Static Scheduling in a Superscalar Processor," ACM SIGARCH Computer Architecture News, ACM Press, Vol. 18, Issue 3, June 1990, pp. 344-354.	
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	NPL58	Smith, M.D. et al., "Limits on Multiple Instruction Issue," Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems, ACM, April 1989, pp. 290-302.	
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	NPL60	Steven, G.B. et al., "HARP: A parallel pipelined RISC processor," Microprocessors and Microsystems, Butterworth & Co. Ltd., Vol. 13, No. 9, November 1989, pp. 579-586.	

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	NPL61	Thornton, J.E., Design of a Computer: The Control Data 6600, Control Data Corporation, 1970, pp. 58-140.	
	NPL62	Tjaden, G.S. and Flynn, M.J., "Detection and Parallel Execution of Independent Instructions," IEEE Transactions On Computers, IEEE, Vol. C-19, No. 10, October 1970, pp. 889-895.	
	NPL63	Tjaden, G.S. and Flynn, M.J., "Representation of Concurrency with Ordering Matrices," IEEE Transactions On Computers, IEEE, Vol. C-22, No. 8, August 1973, pp. 752-761	
	NPL64	Tjaden, G.J., Representation and Detection of Concurrency Using Ordering Matrices, (Dissertation), UMI Dissertation Services, 1972, pp. 1-199.	
	NPL65	Tjaden, G.J., Representation and Detection of Concurrency Using Ordering Matrices, (Dissertation), UMI Dissertation Services, 1972, pp. 1-199.	
	NPL66	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," Proceedings of the 19th Annual Hawaii International Conference on System Sciences, University of Hawaii, IEEE, 1986, pp. 41-50.	
	NPL67	Wedig, R.G., Detection of Concurrency In Directly Executed Language Instruction Streams, (Dissertation), UMI, June 1982, pp. 1-179.	
	NPL68	Weiss, S. and Smith, J.E., "Instruction Issue Logic in Pipelined Supercomputers," IEEE Transactions on Computers, IEEE, Vol. C-33, No. 11, November 1984, pp. 1013-1022 (77-86).	
	NPL69	Baker, T., "Headroom and Legroom in the 80960 Architecture," COMPCON Spring '90: Thirty-Fifth IEEE Computer Society International Conference, IEEE Computer Society, 1990, pp. 299-306.	
	NPL70	Copy of European Search Report from EP Appl. No. 99102406.8, 3 pages, Completed November 24, 1999.	

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